IN THE CLAIMS

Claims 1-5 and 7-16 are pending in the current application. Claims 7, 10, and 15 have been amended. A complete list of the claims as they currently stand is provided below:

1. (Currently amended) An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module, the command sequencer and serializer unit to ~~reduce~~ use a first plurality of address and command signals ~~down to a more narrow set~~ to generate a plurality of signals ~~lines coupled~~ to be input to the memory module, ~~the more narrow set of signal lines forming~~ via a point-to-point interconnect between the command sequencer and serializer unit and the memory module, wherein the plurality of signals is fewer in number than the first plurality of address and command signals.

2. (Original) The apparatus of claim 1, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

3. (Original) The apparatus of claim 2, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

4. (Original) The apparatus of claim 3, each of the plurality of arrays of tag address storage locations organized into 4 ways.

5. (Currently amended) The apparatus of claim 1, the ~~more narrow set~~ plurality of signals ~~lines~~ including a plurality of command and address lines.

6. Cancelled

7. (Currently amended) A memory module, comprising:

a memory device; and

a data cache coupled to the memory device, the data cache controlled by commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations and a command sequencer and serializer unit to use a first plurality of address and command signals to generate a plurality of signals to be input to the memory device, wherein the plurality of signals is fewer in number than the first plurality of address and command signals and the memory controller component is not located on the memory module.

8. (Previously presented) The memory module of claim 7, further comprising a command decoder and deserializer unit to receive command and address information from the memory controller component, the command decoder and deserializer unit providing control for the data cache.

9. (Previously presented) The memory module of claim 8, wherein the data cache is organized into four ways.

10. (Currently amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag

address storage locations to use a first plurality of address and

command signals to generate a plurality of signals, wherein the plurality of

signals is fewer in number than the first plurality of address and command

signals; and

a memory module separate from and coupled to the memory controller via a

memory bus, the memory module including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by

commands delivered by the memory controller.

11. (Previously presented) The system of claim 10, the memory bus including a point-to-point interconnect to couple the memory controller to the memory module.

12. (Original) The system of claim 10, the memory controller further including a plurality of arrays of tag address storage locations.

13. (Original) The system of claim 12, further comprising a plurality of memory modules, each of the plurality of memory modules including at least one of a plurality of memory devices and one of a plurality of data caches, each of the data caches controlled by commands delivered by the memory controller.

14. (Original) The system of claim 13, the plurality of arrays of tag address storage locations and the plurality of data caches organized into four ways.

15. (Currently amended) A method, comprising:

receiving a read request at a memory controller, wherein the memory controller comprises a command sequencer and serializer unit;

generating a plurality of signals from a first plurality of address and command signals using the command sequencer and serializer unit, wherein the plurality of signals is fewer in number than the first plurality of address and command signals;

performing a tag look-up within the memory controller to determine whether there is a cache hit for the read request; and

fetching a line of cache data from a data cache located on a memory module if the tag look-up indicates a cache hit, the memory module separate from the memory controller and coupled to the memory controller via a memory bus.

16. (Original) The method of claim 15, further comprising:

loading a line of data from a memory device located on the memory module to the data cache if the tag look-up indicates a cache miss; and

delivering the line of data to the memory controller.